# Taking silicon quantum dots from lab to 300 mm cmos fabs: recent updates from the imec MOS and Si/SiGe efforts

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In this talk, I will present recent updates from the imec efforts to take silicon quantum dot spin qubits and their control from the laboratory towards fully industrial manufacturing. Over the past years, our effort has focused on optimizing processes and designs to create very low noise [1] and low disorder quantum dots [2] in both MOS and Si/SiGe, in a dedicated effort that entails both thorough gate stack, substrate and control module optimization, as well as efforts to create dedicated cryogenic cmos control modules [3]. The effort entails both fabrication, modeling [4], and cryogenic measurement and validation – the latter both in house and through extended collaborations worldwide.

Recent data on low-disorder, low noise Si MOS quantum dot arrays will be shown, that can be controlled with very high fidelity, as well as results from cryogenic cmos modules that would in principle negate the need for massive amounts of wiring inside the cryostats. Finally, updates will be shown of our approach to developing full back end of line processes in order to further upscale towards larger quantum dot arrays – enabled by advanced optical lithography and heterointegration.

References:

[1] Elsayed et al., Low charge noise quantum dots with industrial CMOS manufacturing, NPJ Quantum 10, 70 (2024)
[2] Elsayed et al., Comprehensive 300 mm process for Silicon spin qubits with modular integration, presented at 2023 IEEE Symposium on VLSI Technology and Circuits (2023)
[3] B. Raes, I. Fattal, A. Caglar et al., *in preparation*
[4] M. Shehata et al., Modeling semiconductor spin qubits and their charge noise environment for quantum gate fidelity estimation, PRB 108, 045305 [2023]