Ingredients for spin-shuttling-based quantum processors in Si/SiGe

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Shuttling based architectures appear promising for overcoming the limitations of dense spin qubit arrays such as crosstalk and wiring density. I will survey progress in realizing the SpinBus architecture [1] in Si/SiGe, which reflects a concrete and realistic proposal for such a design. A key ingredient is the spin-coherent shuttling of electrons in conveyor-mode devices, which need only four control signals independent of distance. Charge transfer works with a fidelity of at least 99.7 ± 0.3 % over a physical distance of 10 µm [2]. Spin-coherent shuttling with a derived fidelity of 99.3 % over about 500 nm limited by nuclear spins in natural Si [3] shows significant improvement in isotopically purified material.

It is expected that valley splitting variations due to alloy disorder are the main limitation for the shuttling speed and fidelity [4]. Valley mapping experiments [5] are consistent with the underlying model for the valley splitting and also support the feasibility of a mitigation approach based on adjusting the shuttling pathway [4].

The realization of such an architecture requires high-yield technology and multiple wiring layers. Largely industrial quantum dot fabrication on 200 mm wafers available with state-of-the-art heterostructure mobilities yields devices with very good stability and noise performance. High charge shuttling fidelities can also be achieved. The available processes meet the requirements for the realization of the spin-bus architecture.

I will also touch on simulation results showing that surface-code based quantum error correction can tolerate surprisingly large shuttling errors as well as experiments demonstrating some ingredients of the for scaling to very large qubit numbers with 3D-integrated cryoelectronic control circuits.

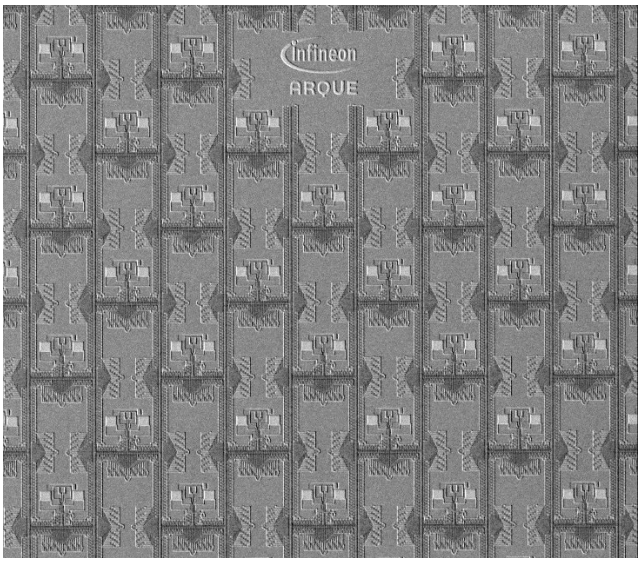

Figure 1, Fabrication test of the of the SpinBus architecture in industrial Si/SiGe technology (without wiring layers)

[1] M. Künne *et al.*, Nat Commun **15**, 4977 (2024).
[2] R. Xue *et al.*, Nat Commun **15**, 2296 (2024).
[3] T. Struck *et al.*, Nat Commun **15**, 1325 (2024).
[4] M. P. Losert *et al.*, arXiv:2405.01832.
[5] M. Volmer *et al.*, Npj Quantum Inf **10**, 61 (2024).